Claims:

1. A system for implementing Incremental Redundancy (IR) operations in a wireless receiver comprising:

at least one processing device that is operable to receive analog signals corresponding to a data block, to sample the analog signals to produce samples, to equalize the samples to produce soft decision bits corresponding to the data block, and to initiate IR operations;

an IR processing function that is operable to perform IR operations on the soft decision bits of the data block in an attempt to correctly decode the data block; and

IR memory operably coupled to the IR processing function, the IR memory including Type I IR memory adapted to store IR status information of the data block and Type II IR memory adapted to store the data block.

2. The system of claim 1, wherein the IR status information stored in Type I IR memory stores retransmission information regarding a corresponding data block sequence number, a Type II IR memory address for each stored data block, and Modulation and Coding Scheme (MCS) mode information for each stored data block.

3. The system of claim 1, wherein the Type II IR memory is adapted to store soft decision bits of the data block, a puncturing pattern of the data block, and a signal quality indicator of the data block.

4. The system of claim 3, wherein Type II IR memory is adapted to store either punctured soft decision bits or depunctured soft decision bits.

5. The system of claim 4, wherein punctured soft decision bits are represented by a first number of soft decision bits per symbol and depunctured soft decision bits are represented by a second number of soft decision bits per symbol, wherein the second number is greater than the first number.

6. The system of claim 4, wherein the punctured soft decision bits are represented by four soft decision bits per symbol and the depunctured soft decision bits are represented by five soft decision bits per symbol.

7. The system of claim 1, wherein the IR memory is adapted to store both segmented data blocks and unsegmented data blocks.

8. The system of claim 1, wherein:

Type I IR memory is statically assigned; and

Type II IR memory is dynamically allocated and deallocated depending upon the requirements of the IR operations.

9. The system of claim 1, wherein Type I IR memory is addressed based upon a block sequence number of the data block.

10. The system of claim 1, wherein at least a portion of the IR processing function comprises an IR processing module distinct from the at least one processing device.

11. The system of claim 1, wherein the at least one processing device comprises a system processor and a baseband processor.

12. The system of claim 1, wherein the IR processing function and the IR memory support Modulation and Coding Scheme (MCS) modes of the GSM EDGE standardized protocol.

13. The system of claim 1, wherein the IR memory is operable to store soft decision bits formed by combining soft decision bits of multiple data blocks.

14. A method for servicing Incremental Redundancy (IR) operations in a wireless receiver comprising:

receiving an analog signal corresponding to a data block;

sampling the analog signal to produce samples;

equalizing the samples to produce soft decision bits corresponding to the data block;

performing IR operations on the soft decision bits of the data block, including decoding the soft decision bits of the data block;

failing to correctly decode the data block;

storing IR status information regarding the data block in Type I IR memory;

allocating Type II IR memory for the data block;

storing an address of the allocated Type II IR memory in Type I IR memory; and

storing at least a portion of the soft decision bits of the data block in the allocated Type II IR memory.

15. The method of claim 14, further comprising:

receiving a second data block;

determining that a Modulation and Coding Scheme (MCS) mode of the second data block is compatible with a MCS mode of the data block;

retrieving soft decision bits of the data block from the allocated Type II IR memory;

combining soft decision bits of the data block with soft decision bits of the second data block to produce combined soft decision bits; and

decoding the combined soft decision bits.

16. The method of claim 15, wherein combining soft decision bits of the data block with soft decision bits of the second data block to produce combined soft decision bits comprises combining punctured soft data bits of the data block with punctured soft data bits of the second data block.

17. The method of claim 15, wherein combining soft decision bits of the data block with soft decision bits of the second data block to produce combined soft decision bits comprises combining depunctured soft data bits of the data block with depunctured soft data bits of the second data block.

18. The method of claim 14, wherein:

each symbol of the data block is represented by four soft decision bits; and

each symbol of the data block is represented by five depunctured soft decision bits.

19. The method of claim 14, further comprising addressing Type I IR memory addressed based upon a block sequence number of the data block.

20. A method for servicing Incremental Redundancy (IR) operations in a wireless receiver comprising:

receiving a data block;

performing IR operations on the data block, including decoding the data block;

failing to correctly decode the data block;

storing IR status information regarding the data block in Type I IR memory;

allocating Type II IR memory for the data block;

storing an address of the allocated Type II IR memory in Type I IR memory; and

storing at least a portion of the data block in the allocated Type II IR memory.

21. The method of claim 20, further comprising:

receiving a second data block;

determining that a Modulation and Coding Scheme (MCS) mode of the second data block is compatible with a MCS mode of the data block;

retrieving soft decision bits of the data block from the allocated Type II IR memory;

combining soft decision bits of the data block with soft decision bits of the second data block to produce combined soft decision bits; and

decoding the combined soft decision bits.

22. The method of claim 21, wherein combining soft decision bits of the data block with soft decision bits of the second data block to produce combined soft decision bits comprises combining punctured soft data bits of the data block with punctured soft data bits of the second data block.

23. The method of claim 21, wherein combining soft decision bits of the data block with soft decision bits of the second data block to produce combined soft decision bits comprises combining depunctured soft data bits of the data block with depunctured soft data bits of the second data block.

24. The method of claim 20, wherein:

each symbol of the data block is represented by four soft decision bits; and

each symbol of the data block is represented by five depunctured soft decision bits.

25. The method of claim 20, further comprising addressing Type I IR memory addressed based upon a block sequence number of the data block.